Remarks

Claims 1-13 are pending in this action. Claims 1-8 and 10-13 stand rejected. Claim 9 is objected to but contains allowable subject matter. Further, by this amendment claims 1, 3, 8-10 and 12 have been amended and reconsideration of all pending claims is respectfully requested.

Claim Rejections - 35 U.S.C. § 103(a), first paragraph

The Examiner rejected claims1-8 and 10-13 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 5,166,926 to Cisneros in view of the paper entitled, "Application Brief: Allayer Rox Bus Architecture," by Allayer Communications.

In regard to independent claims 1, 8 and 10, the Examiner stated that Cisneros discloses the limitations of a switching module for switching LAN traffic in a data transmission system. The first group of limitations cited by the Examiner as being disclosed by Cisneros concerns an input module with a first and a second receiver unit to store a plurality of data packets (1st O.A., p. 4, a and b). Applicants respectfully submit that the input module component of the switching fabric disclosed in Cisneros embodies a fundamentally different approach to improving throughput for packet based switch networks and is inapposite to the input module of Applicant's invention.

First, Applicants' receiving unit corresponds to the select data_in logical circuit 202. (Applicants' Spec. Par. 0022, Figs. 2 and 3) Each select data_in circuit contains eight identical "select data_in" logical blocks 203-1 to 203-8 (Applicants' Spec. Par. 0023, Fig. 2). The select data_in logical blocks include an internal memory 206 and an expansion memory 308. (Applicants' Spec. Par. 0030) In this regard. Applicants' receiver utilizes a dual queue structure whereas Cisneros implements a *single* queue input module to store input packet data (Col. 7, lines 45-51, Col. 21, lines 20-23 and Fig. 5). Applicants' dual queue receiver routes input cells to the internal memory or the expansion memory depending on the value of the destination address

contained in the header of the asynchronous transfer mode (ATM) cell.

The second group of limitations cited by the Examiner as being disclosed by Cisneros concerns an output module that transmits a plurality of user data packets. (1st O.A., p. 4, c and d) Applicants note that the Cisneros output module cooperates with a contention resolution unit to determine the flow of ATM cells through the switching fabric. Since Applicants' receiver allocates input data based on the destination address of the ATM header as noted above, the contention resolution function of the Cisneros input module is obviated in Applicants' switching module design. In addition, the Cisneros interface module prepends a routing header tag to each ATM cell that is used solely within the switch. (Col. 7, lines 38-41) The routing header tag disclosed in Cisneros overwrites the virtual channel identifier (VCI) field of the ATM cell header and specifies a physical output module address and a specific output port address on that output module to which that cell is destined. (Col. 7, lines 41-45)

Conversely, Applicants' system expressly avoids changing the packet address when it is necessary to change a switch module routing. (Applicants' Spec. Para. 0044) In other words, the routing of data packets to their final destination is done without modifying the data packet header. (Applicants' Abstract) Instead, Applicants assign a range of legal address values for each switch module and route received data packets, based on this assignment, to either the internal memory location or an expansion memory location of the data_in logical block. Accordingly, Cisneros neither suggests nor motivates the data packet ranging and detection system disclosed by Applicants. Indeed, Cisneros teaches away from Applicants' approach because the invention herein requires no modification of the ATM cell header. Thus, the output function of Cisneros is implemented in an entirely different manner then Applicants' invention.

The third limitation cited by the Examiner is directed to a self routing cross point plane

switch or "crossbar switch." (1st O.A., p. 5, e) used to route the data to the output modules. Cisneros employs a cell address "look ahead" feature that relies on storing configuration information within each cross-point circuit in every cross point, in every cross point switching plane, one cell in advance of the actual that is being routed therethrough. (Col. 8, lines 7-11) However, Applicants realize the crossbar function without the look ahead feature. Similarly, the Self-Routing Cross Point Plane switch disclosed by Cisneros does not suggest or motivate the cross bar switch of Applicants' invention because the routing function in Cisneros is achieved using the prepended ATM header tag and the cell look ahead feature.

In connection with the limitation recited in claim 8, regarding the coupling of multiple switching modules, the Examiner cited Cisneros in combination with a paper titled "Application Brief: Allayer RoX Bus Architecture," by Allayer Communications. Applicants respectfully submit that the Allayer Communications reference is directed to an ATM switching architecture known in the art as a Ring of Switches (RoX) and specifically discredits crossbar switch based architectures as being inefficient and not well suited for Ethernet applications. (Allayer's RoX Bus Architecture, pp. 3-5) As such, the Allayer reference expressly teaches away from Applicants' methodology, which is specifically directed to crossbar switch based Ethernet or token ring ATM applications. (Applicants' Spec. Par. 10) Further, to establish a prima facie case of obviousness some motivation to combine Cisneros and Allayer must be found in the prior art. (MPEP §2143.01) Since Allayer recites a list of disadvantages of crossbar based switching modules there is no motivation to combine the reference with Cisneros and no prima facie case of obviousness has been established.

Although Applicants' receiver circuit is not motivated or suggested by the single queue input module of Cisneros, Applicants have amended claims 1, 8 and 10 to include a limitation

describing the dual queue (memory) of the input module receiver. Therefore Applicants respectfully submit that the rejection of claims 1, 8 and 10 under 35 U.S.C. § 103(a) has been overcome.

In regard to claim 2, the Examiner indicated that the first and second memory elements recited are rendered obvious in view of the buffer memory corresponding to a particular input module of Cisneros. As noted above, Cisneros discloses a single queue input module rather than the dual queue (memory) approach claimed by Applicants.

The Examiner also indicated that the selector unit contained within Applicants' select data_in logical block is obvious in view of the multiplexor disclosed in Cisneros. However, Applicants respectfully submit that the time division multiplexing Cisneros performs on the input data stream is not analogous to the selector unit of Applicants' select data_in logical block, which routes the input ATM cell to the internal memory or the expansion memory based on the final destination address included in the ATM header. As such, Cisneros does not suggest the structure and function of the selector unit.

Therefore, Applicants respectfully submit that the rejection of claim 2 under 35 U.S.C. § 103(a) has been overcome.

In regard to claims 3, 6 and 7 the Examiner stated that Cisneros further discloses prepending a switch routing header to each received ATM cell and therefore the recitation of an additional byte to define the final destination of the data packet in claim 3 was obvious in view of Cisneros. However, as noted above, no change to the ATM header is required for Applicants' invention. The final destination address and module bit configuration fields of the ATM header

are part of the standard ATM format. Accordingly, claim 3 has been amended to remove any ambiguity regarding the final destination address and module bit configuration fields of the data packet specified in the ATM header.

Claim 6 recites an "address configurator" used to predefine the address of the switching module, which refers to the selected range of final destination addresses that the switching module will accept for internal memory storage. The address configurator limitation is not directed toward editing the final destination address defined in the ATM header but is instead an internal mechanism for system initialization. Similarly, claim 7 recites a bit configuration of the switching module that is compared with the module bit configuration of each input data packet. Applicants respectfully submit that the bit configuration of claim 7 refers to a comparison with the preexisting module bit configuration contained in the header of the incoming ATM data packet (cell).

Accordingly, none of the elements recited in claims 3, 6 or 7 are obvious in view of Cisneros. In addition, Claim 3 depends on claim 2, which is dependent on claim 1 as amended; claim 6 depends on claim 1 as amended; and claim 7 depends on claim 6, which depends on claim 1 as amended. Therefore, Applicants respectfully submit that the rejection of claims 3, 6 and 7 under 35 U.S.C. § 103(a) has been overcome.

The Examiner rejected claims 4 and 5 under 35 U.S.C. § 103(a) as being unpatentable over Cisneros. Claims 4 and 5 depend on claim 2, which is dependent on claim 1 as amended. Therefore, Applicants respectfully submit that the rejection of claims 4 and 5 under 35 U.S.C. § 103(a) has been overcome.

The Examiner rejected claim 11 under 35 U.S.C. § 103(a) as being unpatentable over Cisneros. Claim 11 depends on claim 10 as amended. Therefore, Applicants respectfully submit that the rejection of claim 11 under 35 U.S.C. § 103(a) has been overcome.

The Examiner rejected claims 12 and 13 under 35 U.S.C. § 103(a) as being unpatentable over Cisneros in view of Allayer. As noted in the remarks directed to claims 1, 8 and 10, Applicants' receiver utilizes a dual queue structure whereas Cisneros implements a *single* queue input module to store input packet data (Col. 7, lines 45-51, Col. 21, lines 20-23 and Fig. 5). Applicants' dual queue receiver routes input cells to the internal memory or the expansion memory depending on the value of the destination address contained in the header of the asynchronous transfer mode (ATM) cell.

Applicants note that the routing header tag disclosed in Cisneros overwrites the virtual channel identifier (VCI) field of the ATM cell header and specifies a physical output module address and a specific output port address on that output module to which that cell is destined. (Col. 7, lines 41-45) Conversely, Applicants' system expressly avoids changing the packet address when it is necessary to change a switch module routing. (Applicants' Spec. Para. 0044) Applicants assign a range of legal address values for each switch module and route received data packets, based on this assignment, to either the internal memory location or an expansion memory location of the data_in logical block.

Finally, to establish a prima facie case of obviousness some motivation to combine Cisneros and Allayer must be found in the prior art. (MPEP §2143.01) Since Allayer recites a list of disadvantages of crossbar based switching modules there is no motivation to combine the reference with Cisneros and no prima facie case of obviousness has been established.

Accordingly, Applicants have amended Claim12 to add a limitation regarding the dual queue (memory) structure of the data_in selector logical blocks. Claim 13 depends on claim 12 as amended. Therefore, Applicants respectfully submit that the rejection of claims 12 and 13 under

35 U.S.C. § 103(a) has been overcome.

Allowable Subject Matter

The Examiner objected to claim 9 as being dependent upon a rejected base claim, but indicated that claim 9 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicants have amended claim 9 to be in independent form with all the limitations of the original base claim 8 and respectfully submit that claim 9 as amended is now in condition for allowance. Therefore, Applicants respectfully submit the Examiner's objection to claim 9 has been overcome.

Conclusion

Based on the foregoing, it is respectfully submitted that the pending claims in the subject patent application are in condition for allowance and that the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully submitted,
For: Alain Benayoun, et al.

By: _____

Michael J. LeStrange
Registration No. 53,207
Telephone No.: (802) 769-1375
Fax No.: (802)769-8938
EMAIL: lestrange@us.ibm.com

International Business Machines Corporation
Intellectual Property Law - Mail 972E
1000 River Road
Essex Junction, VT 05452